IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	DAVID K. VAVRO	§ Group Art Unit:	
Serial No.:	Not Assigned	§	
Filed:	April 4, 2001	§ Examiner:	
For:	DATA DRIVEN DIGITAL SIGNAL PROCESSOR	§ Atty. Dkt. No.:	INTL-0546-US (P11105)

Box PATENT APPLICATION
Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Please amend the above-referenced application.

In the Specification:

Replace the paragraph on page 6, starting at line 27, with the following:

The architecture shown in Figure 1 is simply an example of one potential architecture. The number of input processors 12a and output processors 12b may vary from one to several. The number of memory processors 12c is also considerably variable. Likewise, the number and arrangement of the MAC processors 12e, or add and subtract processors 12d may likewise be subject to considerable variability. Other processing elements 12 (not illustrated) may be combined as well.

Replace the paragraph on page 7, starting at line 15, with the following:

Instructions are executed by any given processing elements 12 when all the necessary data is currently available in a general purpose register 32 as indicated by the data valid bits 36. Storage of the result of instruction execution by a given processing element 12 occurs when space is available in a general purpose register 32 (unless the results of the instruction do not target a register 32). Thus, the multi-processing environment is a data driven, shared register with a peer-to-peer architecture using a multiple instruction, multiple data type digital signal processor 10.

Replace the paragraph on page 11, starting at line 12, with the following:

The advantages over a non-data driven architecture may include, in some embodiments, providing an architecture that can adapt to the addition of new processing elements without affecting preexisting code. Expanding the number of data valid bits may have no affect, in some embodiments, because the data valid bits that do not get set do not get used. This assumes that the encoding of the instruction is such that the old instruction fits inside the new instruction space and the new data valid control bits are not utilized. A purely data driven instruction execution model, in one embodiment, allows software to be functional, hardware timing independent and thus portable across different silicon processing technologies. Binary assembly code written on one version of the digital signal processor 10 may be portable across other processors that have different types or versions of the same processing elements.

Remarks

The Assistant Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Respectfully submitted,

Date: 4/4/01

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VERSION WITH MARKINGS TO SHOW CHANGES

The paragraph on page 6, starting at line 27, has been revised as follows:

The architecture shown in Figure 1 is simply an example of one potential architecture. The number of input processors 12a and output processors 12b may vary from one to several. The number of memory processors 12c is also considerably variable. Likewise, the number and arrangement of the MAC processors [12d] 12e, or add and subtract processors [12e] 12d may likewise be subject to considerable variability. Other processing elements 12 (not illustrated) may be combined as well.

The paragraph on page 7, starting at line 15, has been revised as follows:

Instructions are executed by any given processing elements 12 when all the necessary data is currently available in a general purpose register 32 as indicated by the data valid bits 36. Storage of the result of instruction execution by a given processing element 12 occurs when space is available in a general purpose register 32 (unless the results of the instruction do not target a register 32). Thus, the multi-processing environment is a data driven, shared [memory] register with a peer-to-peer architecture using a multiple instruction, multiple data type digital signal processor 10.

The paragraph on page 11, starting at line 12, has been revised as follows:

The advantages over a non-data driven architecture may include, in some embodiments, providing an architecture that can adapt to the addition of new processing elements without affecting preexisting code. Expanding the number of data valid bits may have no affect, in some embodiments, because the data valid bits that do not get set do not get used. This assumes that the encoding of the instruction is such that the old instruction fits inside the new instruction space and the new data valid control bits are not utilized. A purely data driven instruction execution model, in one embodiment, allows software to be functional, hardware timing independent and thus portable across different silicon processing technologies. Binary assembly code written on one version of the digital signal processor 10 may be portable across other processors that have different types or versions of the same processing elements.